

## **PA69**





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## **FEATURES**

- A UNIQUE (Patent Pending) TECHNIQUE FOR VERY LOW QUIESCENT CURRENT
- OVER 350 V/µS SLEW RATE
- WIDE SUPPLY VOLTAGE
  - Single Supply: 20V to 200V
  - Split Supplies: +/- 10V to +/- 100V
- OUTPUT CURRENT- 75mA cont.; 100mA Pk
- UP TO 23 WATT DISSIPATION CAPABILITY
- OVER 200 kHz POWER BANDWIDTH

## **APPLICATIONS**

- PIEZOELECTRIC POSITIONING AND ACTUATION
- ELECTROSTATIC DEFLECTION
- DEFORMABLE MIRROR ACTUATORS
- CHEMICAL AND BIOLOGICAL STIMULATORS

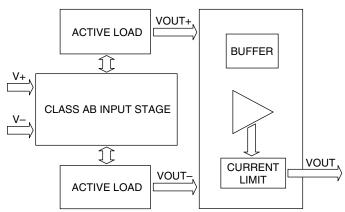
#### **DESCRIPTION**

The PA69 is a high voltage, high speed Precision IC power op amp with performance and unique features not found previously in any commercially available OpAmp.

Novel input stage design of this amplifier provides extremely high slew rates in pulse applications while maintaining low quiescent current of under 1mA. This novel input stage also has the effect of adding variables to the power response and slew rate characteristics of the amplifier. To a lesser degree, there are also input related effects on unity gain bandwidth and phase. It is important to note that the slew rate is a strong function of input voltage amplitude. It should be noted that the package tab needs to be connected to a stable reference such as GND for high slew rates. Please refer to special considerations section for details.

The output stages are well protected with user defined current limit although the Safe Operating Area (SOA) must be observed for reliable protection. Proper heatsinking is required for maintaining maximum reliability. External phase compensation provides the user with great flexibility in trading gain, stability and bandwidth.

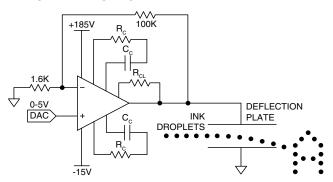
## **BLOCK DIAGRAM**





12-PIN SIP PACKAGE STYLE EU LEAD FORM EW

## TYPICAL APPLICATION



The PA69 is ideally suited to driving continuous drop ink jet systems, in both piezo actuation and deflection applications. The deflection amplifier shown above achieves accurate droplet displacement at high speeds to deposit crisp, clear lot code information on product containers. The external compensation networks have been optimized to match the gain of the circuit and the complex impedance of the load. The combination of high voltage and high speed allow repeatable low cost deflection of droplets for high production environments.

# **PA69**

#### **ABSOLUTE MAXIMUM RATINGS**

SUPPLY VOLTAGE, +V  $_{\rm S}$  to -V  $_{\rm S}$  OUTPUT CURRENT, peak (200ms) 200V 200mA, within SOA POWER DISSIPATION, internal, DC 23W INPUT VOLTAGE, Differential ±15V INPUT VOLTAGE, Common Mode ±Vs TEMPERATURE, pin solder, 10s, EU 260°C TEMPERATURE, junction<sup>2</sup> 150°C. TEMPERATURE RANGE, storage -55 to 125°C OPERATING TEMPERATURE, case -40 to 125°C

## **SPECIFICATIONS**

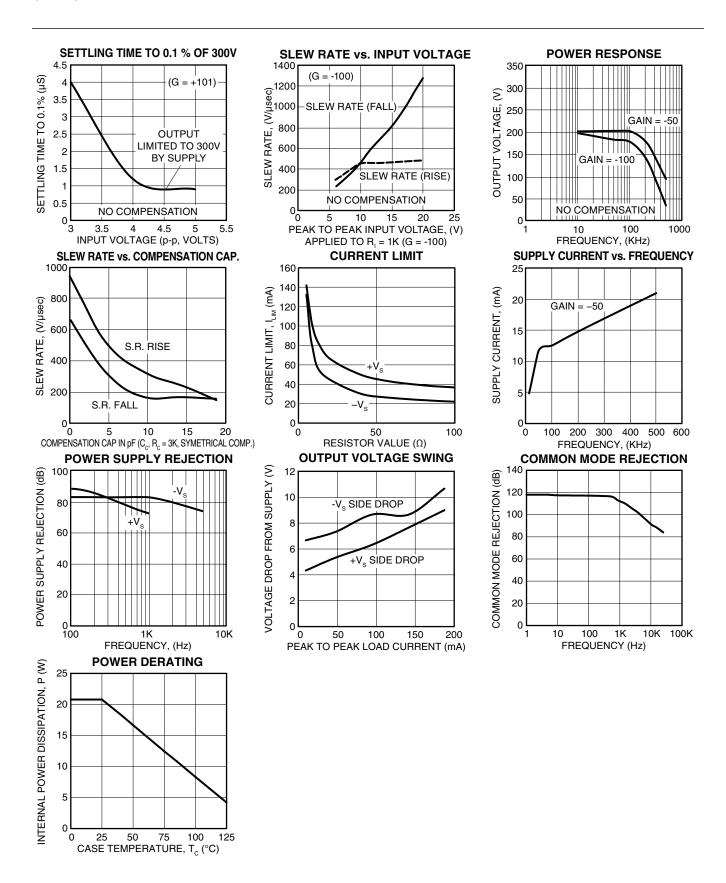
PARAMETER	TEST CONDITIONS <sup>1</sup>	MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE OFFSET VOLTAGE vs. temperature OFFSET VOLTAGE vs. supply BIAS CURRENT, initial OFFSET CURRENT, initial	0 to 125°C (CaseTemperature)	-25	8 -63 8.5 12	25 32 200 400	mV μV/°C μV/V pA pA
INPUT RESISTANCE, DC COMMON MODE VOLTAGE RANGE, pos. COMMON MODE VOLTAGE RANGE, neg. COMMON MODE REJECTION, DC NOISE NOISE, V <sub>O</sub> NOISE	700KHz	90	10 <sup>8</sup> +V <sub>s</sub> - 2 -V <sub>s</sub> + 5.5 118 418 500		Ω V V dB μV RMS nV/√Hz
GAIN OPEN LOOP @ 1Hz GAIN BANDWIDTH PRODUCT @ 1MHz PHASE MARGIN	Full temperature range	89	120 1 50		dB MHz
OUTPUT  VOLTAGE SWING  VOLTAGE SWING  CURRENT, continuous, DC  SLEW RATE  SETTLING TIME, to 0.1%  POWER BANDWIDTH, 300V <sub>P-P</sub> OUTPUT RESISTANCE, No Load	$I_{o} = 10\text{mA}$ $I_{o} = 75\text{mA}$ Package Tab Connected to GND 5V Step (No Compensation) $+V_{s} = 160\text{V}, -V_{s} = -160\text{V}$ $R_{cL} = 6.2\Omega$	75 100	IV <sub>s</sub>   - 2   IV <sub>s</sub>   - 8.6   350   1   200   44	V <sub>s</sub>   – 12	V V mA V/μS μS kHz
POWER SUPPLY VOLTAGE CURRENT, quiescent <sup>5</sup>	±100V Supply	±10 0.2	±50 0.7	±100 2.5	V mA
THERMAL RESISTANCE, DC, junction to case RESISTANCE, junction to air TEMPERATURE RANGE, case	Full temperature range Full temperature range	-40	5.5 12.21	125	°C/W °C/W

NOTES: 1. Unless otherwise noted:  $TC = 25^{\circ}C$ , DC input specifications are  $\pm$  value given, power supply voltage is typical rating.

3.  $+\vec{V}_s$  and  $-\vec{V}_s$  denote the positive and negative supply voltages of the output stage.

- 4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
- 5. Supply current increases with signal frequency. See graph on page 4.

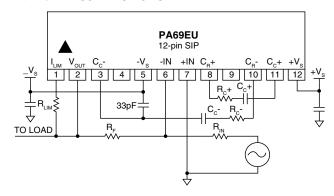
<sup>2.</sup> Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve



OPERATING CONSIDERATIONS

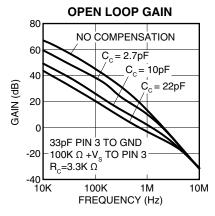
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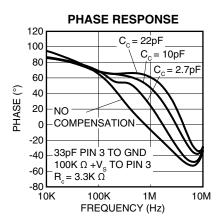
#### EXTERNAL CONNECTIONS



### **SMALL SIGNAL GAIN AND PHASE PLOTS**

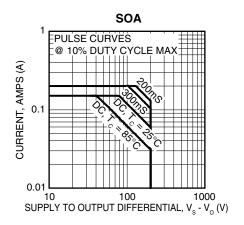
The input signal amplitude to the PA69 amplifier is related to the overall phase margin and unity gain bandwidth. For very small signal amplitudes the amplifier phase margin is negative and it shows instability. If small signal stability is desired a constant current source of 500 uA (or resistor for constant supply voltage) needs to be added externally between  $C_c$ - and + $V_s$ .  $\stackrel{\scriptstyle \leq}{\underset{\scriptstyle \sim}{\stackrel{\scriptstyle \sim}{\stackrel{\sim}{\stackrel{\sim}}{\stackrel{\sim}{\stackrel{\sim}}{\stackrel{\sim}{\stackrel{\sim}}{\stackrel{\sim}{\stackrel{\sim}}{\stackrel{\sim}}{\stackrel{\sim}{\stackrel{\sim}}{\stackrel{\sim}}}}}}$  This current source has minor effects on output to be added externally between  $C_c$  – and + $V_s$ . offset voltage but helps immensely with small signal stability. The following gain and phase plots have been generated with a 100k resistor (fixed dual supply voltage +/- 50V) between C<sub>c</sub>- and +V<sub>s</sub>. Please note that the unity gain bandwidth and phase margin improves with larger signal amplitude because of the unique differential amplifier stage in the PA69.





## SAFE OPERATING AREA

The MOSFET output stage of the PA69 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA. The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast–recovery diodes must be used.



OPERATING CONSIDERATIONS PA69

#### **GENERAL**

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit <a href="https://www.apexmicrotech.com">www.apexmicrotech.com</a> for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

#### SPECIAL CONSIDERATIONS

It is very important to realize that in order to achieve high frequency performance the heat sink tab has to be tied to a stable, low impedance reference, i.e. power supply or GND. An AC connection through a 0.1µF capacitor is also sufficient. Internal to the PA69, the heatsink tab is electrically isolated to more than 350V. This may help allay some electrical isolation concerns in tying the heat sink to Vs or GND.

## **CURRENT LIMIT**

For proper operation, the current limit resistor,  $R_{\rm LIM}$ , must be connected as shown in the external connections diagram. For maximum reliability and protection, the resistor should be set as high as possible. The maximum practical value using the following formula is 12 ohms. For even lower current limit values, please see the CURRENT LIMIT vs. RESISTOR graph on the TYPICAL PERFORMANCE GRAPHS page.

$$R_{LIM} = 0.7 / I_{LIM}$$

#### POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals +Vs and –Vs must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PA69. Use high quality ceramic capacitors (X7R) 0.1µF or greater.

#### **SUPPLY CURRENT**

The PA69 features a class A/B driver stage to drive the output MOSFETs and an innovative input stage to achieve very high slew rates. The supply current drawn by the PA69, even with no load, varies with the slew rate of the output signal.

### **STABILITY**

The PA69 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. Due to the innovative design of the PA69, two compensation networks are required. The values of these components should be the same to provide symmetric slew rate characteristics. The compensation capacitor Cc must be rated at 500V working voltage. NPO capacitors are recommended. The compensation networks CcRc must be mounted closely to the amplifier pins 8 & 11 and 3 & 10 to avoid spurious oscillation.

The PA69 may require an external 33 pF capacitor (minimum breakdown of 350V) between Cc– and –Vs to prevent oscillations in the falling edge of the output. This capacitor is provided with the evaluation kit. Please refer to EK60U datasheet for details.

## **ELECTROSTATIC DISCHARGE**

Like many high performance MOSFET amplifiers, the PA69 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.